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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/699,473	10/31/2003	Jonghee Han	2003P52883US	2763

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EXAMINER	
HASSAN, AURANGZEB	

ART UNIT	PAPER NUMBER
2182	

DATE MAILED: 01/17/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/699,473	HAN, JONGHEE	
	Examiner	Art Unit	
	Aurangzeb Hassan	2182	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 October 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-42* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-42* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *31 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *5/4/2005*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claim 41 is objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form. In reference to claim 39, claim 41 is rather restating the stipulations set forth in its dependency without any further limiting functionality and therefore object to by the examiner.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1 – 42 are rejected under 35 U.S.C. 102(b) as being anticipated by Park (US Patent Number 6,147,926).

4. As per claims 1, 10, 16, 18, 23, 26, 27, 29, 39 Park teaches a method and device comprising,

a bidirectional data bus (element 105, figure 1);

a first driver circuit coupled to the bus (FRDB, column 4, lines 40 – 42) and configured to propagate a first data and a second data in a first direction along the bus;

a first receiver circuit coupled to an end of the bus opposite the first driver circuit and configured to latch (FRDB latch, element 41, figure 2, column 4 line 39) the first and second data in response to a first strobe clock signal (FRDB strobe signal, column 4, lines 40 – 42);

a second driver circuit coupled to the bus (SRDB, column 4, lines 43 – 44) and configured to propagate a third data and a fourth data in a second direction along the bus;

a second receiver circuit coupled to an end of the bus opposite the second driver circuit and configured to latch (SRDB latch, element 42, figure 2, column 4, line 47) the third and fourth data in response to a second strobe clock signal;

a first controller configured to enable the first driver circuit and to generate the first strobe clock signal (first Enable, column 7 lines 1 – 16);

a second controller configured to enable the second driver circuit and to generate the second strobe clock signal (second Enable, column 7 lines 1 – 16);

a first strobe clock signal line (FRDB strobe signal, column 4, lines 40 – 42) to propagate the first strobe clock signal from the first controller to the first receiver circuit;

a first round-trip path comprising a first return path for the first strobe clock signal back to the first controller (column 6, 42 – 60, controller round- trip path);

a second strobe clock signal line (SRDB strobe signal, column 4, lines 43 – 45) to propagate the second strobe clock signal from the second controller to the second receiver circuit; and

a second round-trip path comprising a second return path for the second strobe clock signal back to the second controller (column 6, 42 – 60, controller round- trip path).

5. As per claim 2, Park teaches a method wherein driving the first data and the second data on the data bus comprises enabling a driver to drive the data (output driver, element 44, figure 2, column 4, lines 55 – 65).

6. As per claims 3 and 22, Park teaches a method wherein the data bus is an internal data bus of the multiple data rate memory device (column 4, lines 1 – 20).

The data bus taught by Park is internal to the DDR SDRAM thus internal to the memory device.

7. As per claims 4, 15, 24, 31, Park teaches a method wherein the multiple data rate memory device is a double data rate synchronous dynamic random access memory (DDR SDRAM) (DDR SDRAM, column 4, lines 14 – 16).

8. As per claims 5, 19, 30, Park teaches a method wherein a duration of time between issuing the strobe signal and receiving the return signal is at least as long as a duration of time required for the strobe signal to propagate from the control circuit to the receiving circuit (element 33, figure 2, column 4, lines 63 – 65).

9. As per claims 6 and 20, Park teaches a method wherein; a duration of time between issuing the strobe signal and receiving the return signal is substantially equal to a duration of time required for the strobe signal to propagate from the control circuit to the receiving circuit (element 33, figure 2, column 5, lines 1 – 7).

10. As per claim 7, Park teaches a method wherein the return signal is the strobe signal (column 4, lines 40 – 48, strobe signals).

11. As per claim 8, Park teaches a method further comprising generating the return signal by the receiving circuit (column 6, lines 27- 29 & 45 – 53).

12. As per claim 9, Park teaches a method wherein generating the return signal comprises buffering the strobe signal (output buffer, element 44, figure 2, column 5, lines 12 – 17).

13. As per claim 11, Park teaches a method wherein (a)-(f) are performed bidirectionally over the data bus (element 105, figure 1).

14. As per claims 12, 17, 25, Park teaches a method wherein the strobe signal is propagated to the receiving circuit on a first path and propagated to the controller on a second path, and wherein only a portion of each path shares a common line (database controlling unit, element 34, figure 2, column 6, lines 38 – 61).

Database controlling unit taught by Park, tied into the FIFO unit element 35 of figure 2 and the latency pipeline controlling unit element 36 of figure 2 allow for sharing a common line in a portion.

15. As per claim 13, Park teaches a method wherein the strobe signal is propagated to the receiving circuit on a first path and propagated to the controller on a second path, and wherein lengths of the first and second paths are substantially the same (column 6, lines 50 – 67).

16. As per claim 14, Park teaches a method comprising, latching the second data in from the data bus (SRDB latch, element 42, figure 2, column 4, line 47).

17. As per claim 21, Park teaches a method wherein receiving the strobe signal by the control circuit occurs substantially simultaneously with receipt of the strobe signal by the receiving circuit (database controlling unit, element 34, figure 2, column 6, lines 39 – 53).

18. As per claim 28, Park teaches a device wherein the round-trip path is partially defined by the strobe clock signal line (column 6, 42 – 60, controller round- trip path).

19. As per claim 32, Park teaches a circuit comprising:

a controller comprising a strobe clock signal output (strobe signal, column 4, lines 40 – 45) and a return clock signal input and configured to issue a first enable signal (first Enable, column 7 lines 1 – 16) and a second enable signal (second Enable, column 7 lines 1 – 16), the first enable signal enabling a plurality of drivers to drive respective first data on respective data lines, and the second enable signal enabling the plurality of drivers to drive respective second data on their respective data lines;

a strobe clock signal line coupled to the strobe clock signal output (SDO, column 4, lines 45 – 50); and

a return clock signal line coupled to the return clock signal input; wherein the strobe clock signal line defines an initial portion of a round-trip path and the return clock signal line defines a terminal portion of the round-trip path; and wherein the controller is configured to (column 5, lines 20 – 26);

respond to an external clock signal by pulling a strobe clock signal to a first state on the strobe clock signal line and pulling the first enable signal to an active state (column 7, lines 1 – 10);

receive a return clock signal on the return clock signal line a period of time after pulling the strobe clock signal to the first state, wherein the return clock

signal is timed off of the strobe clock signal and indicates an assumed receipt of the strobe clock signal in the active state by receiving circuitry coupled to the respective data lines and configured to latch in the first (FRDB latch, element 41, figure 2, column 4 line 39) and second (SRDB latch, element 42, figure 2, column 4, line 47) data from the data lines in response to the strobe clock signal; and

respond to the received return clock signal by pulling the second enable signal to an active state (column 7, line 4).

20. As per claim 33, Park teaches a circuit wherein the multiple data rate memory device is a double data rate synchronous dynamic random access memory (DDR SDRAM, column 4, lines 14 – 16).

21. As per claim 34, Park teaches a circuit wherein the strobe clock signal is coupled to the return clock signal line and to the receiving circuitry (elements 41 and 42, figure 2, coupled to F/SRDB for receiving).

22. As per claim 35, Park teaches a circuit wherein the receiving circuitry is configured to latch (FRDB latch, element 41, figure 2, column 4 line 39) in the first data from the data lines in response to receiving the strobe clock signal in the first state and to latch (SRDB latch, element 42, figure 2, column 4, line 47) in the second data from the data lines in response to receiving a transition of the strobe clock signal from the first state to a second state.

23. As per claim 36, Park teaches a circuit wherein the return clock signal is a delayed instance of the strobe clock signal (element 33, figure 2, column 4, lines 60 – 65).

24. As per claim 37, Park teaches a circuit wherein the strobe clock signal and the return clock signal are issued within a single period of an external clock signal (element 33, figure 2, column 5, lines 19 - 29).

25. As per claim 38, Park teaches a circuit wherein the return clock signal is a delayed instance of the strobe clock signal (element 33, figure 2, column 4, lines 55 – 65).

26. As per claim 40, Park teaches a device wherein the first round-trip path is partially defined by the first strobe clock signal line (FRDB strobe signal, column 4, lines 40 – 42) and the second round-trip path is partially defined by the second strobe clock signal line (SRDB strobe signal, column 4, lines 43 – 45).

27. As per claim 41, Park teaches a device wherein:

the first controller is configured to enable (first Enable, column 7 lines 1 – 16)the first driver circuit to drive the first data on the data bus (FRDB, column 4, lines 40 – 42), generate the first strobe clock signal (FRDB strobe signal, column 4, lines 40 – 42)

propagated to the first receiver circuit on the first strobe clock signal line, receive the first strobe clock signal on the first round-trip path and, in response to receiving the first strobe clock signal, enable the first driver circuit to drive the second data on the data bus; and

the second controller is configured to enable (second Enable, column 7 lines 1 – 16)the second driver circuit to drive the third data on the data bus (SRDB, column 4, lines 43 – 44) , generate the second strobe clock signal (SRDB strobe signal, column 4, lines 43 – 45) propagated to the second receiver circuit on the second strobe clock signal line, receive the second strobe clock signal on the second round-trip path and, in response to receiving the second strobe clock signal, enable the second driver circuit to drive the fourth data on the data bus (elements 47, 48, 57, 60, figure 4, column 5, lines 30 – 50)

28. As per claim 42, Park teaches a device wherein the first strobe clock signal line comprises at least a portion of the second strobe clock signal line (database controlling unit, element 34, figure 2, lines 35 – 50).

Conclusion

29. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Aurangzeb Hassan whose telephone number is (571)272-8625. The examiner can normally be reached on Monday - Friday 9 AM to 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kim Huynh can be reached on (571)272-4147. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

AH
1/6/2006

KIM HUYNH
SUPERVISORY PATENT EXAMINER
1/9/06